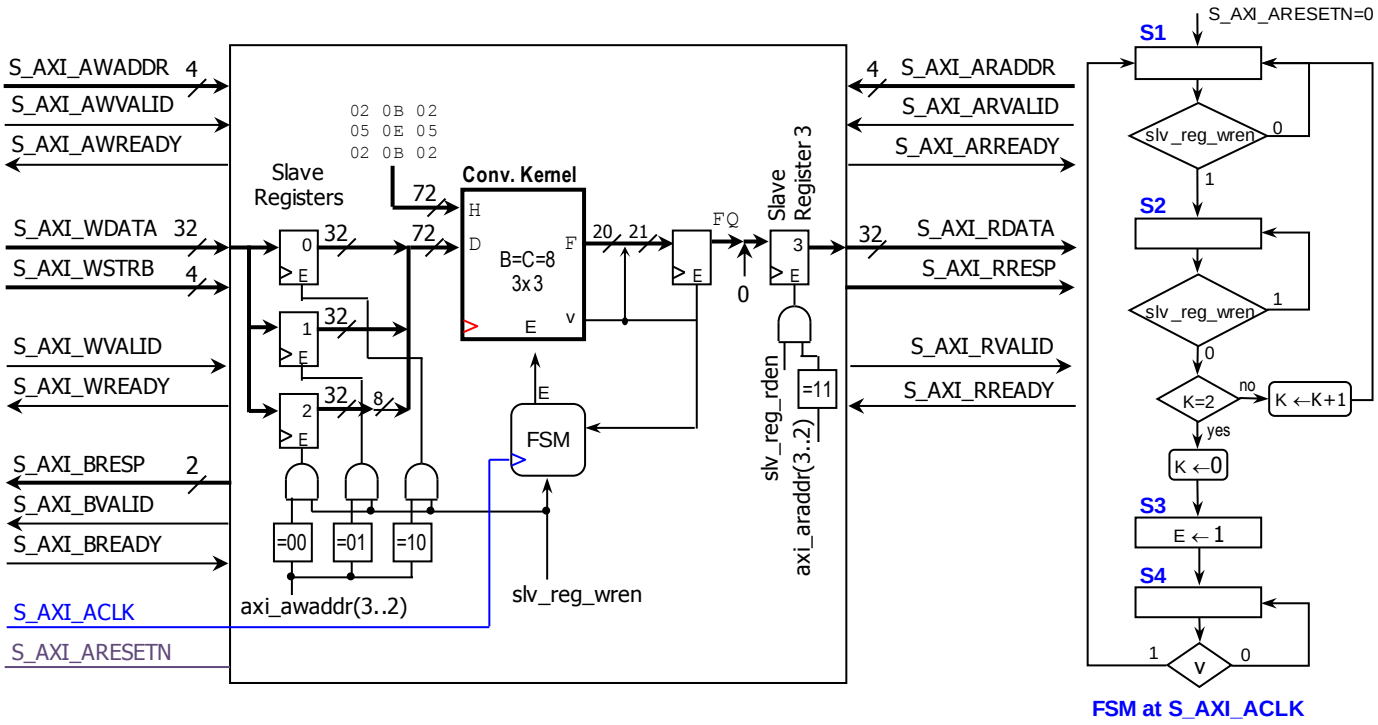
Homework 3

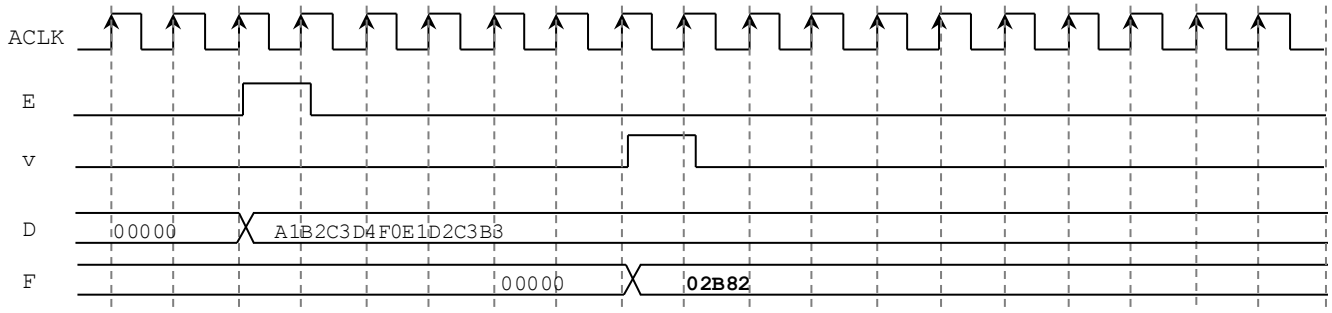
(Due date: November 7th @ 5:30 pm)

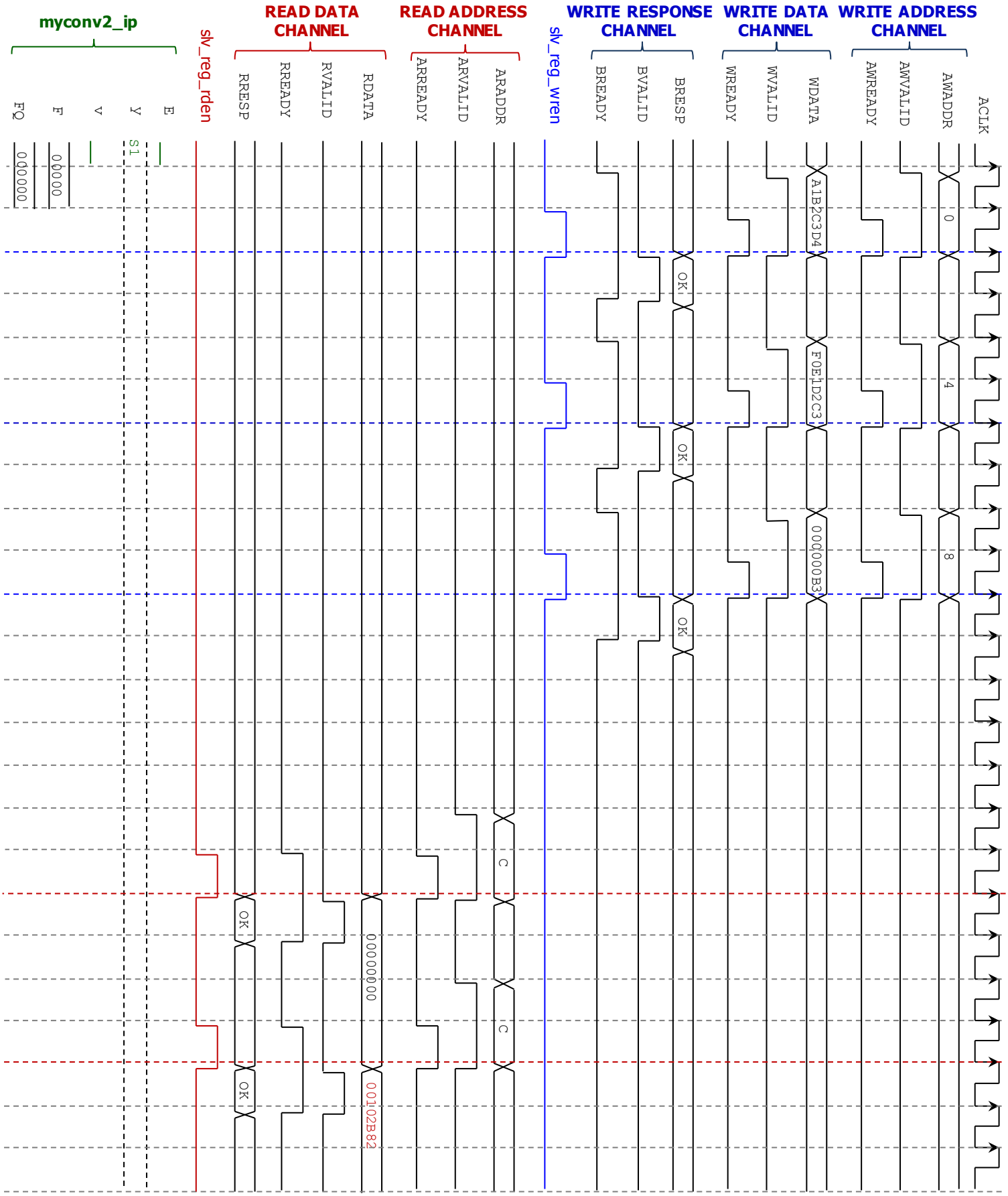
Presentation and clarity are very important! Show your procedure!

PROBLEM 1 (15 PTS)

- AXI4-Lite interface: The following is the interface for the pipelined 2D convolution kernel. The input/output timing diagram of the pipelined 2D convolutional kernel is shown below. For the input data (`0xA1B2C3D4F0E1D2C3B3`), the result is `0x2B282` and it appears 6 clock cycles after *E* is asserted.
  - ✓ Given the AXI signals, complete the timing diagram of the signals corresponding to the 2D Convolution Kernel block (`E, v, y, F, FQ` signals) on the next page.

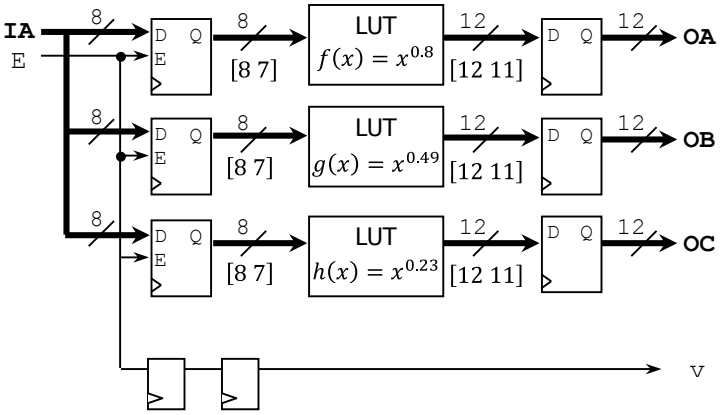





myconv2_ip
FQ
F
v
y
E
S1
sv_reg_rden
READ DATA CHANNEL
RRESP
RREADY
RVALID
RDATA
READ ADDRESS CHANNEL
ARREADY
ARVALID
ARADDR
sv_reg_wren
WRITE RESPONSE CHANNEL
BREADY
BVALID
BRESP
WRITE DATA CHANNEL
WREADY
WVALID
WDATA
WRITE ADDRESS CHANNEL
AWREADY
AWVALID
AWADDR
ACLK
OK
A1B2C3D4
F0E1D2C3
00000B3
C
00000000
00102B82
0
4
8

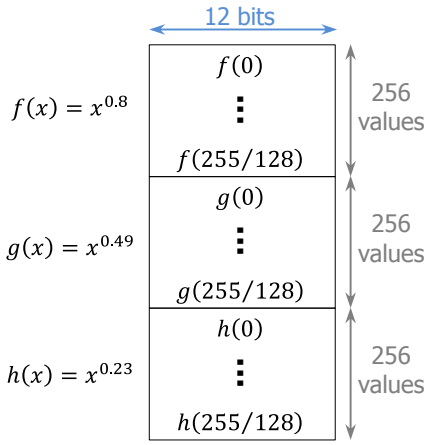
PROBLEM 2 (85 PTS)

- Implement the following circuit using the LUT approach.
  - ✓ Input format: [8 7] (unsigned)
  - ✓ Output format: [12 11] (unsigned)



- Pre-compute the LUT values and store them as binary numbers in a text file. You can use the MATLAB script `LUTvalGen8to12.m` to do this. Your VHDL code should read the text file.

- The text file should be divided as follows: the first 256 entries for the first function, the second 256 entries for the second function, and the third 256 entries for the third function:



SIMULATION

- Create a testbench to test your circuit. The testbench must generate all the possible input cases (from 00000000 to 11111111) and write the output results in a text file. For simplicity's sake, it is suggested that you write three 12-bit words per line (256 lines), where each 12-bit word represents the output of a different function.
- To verify the correct operation of your circuit, compare the text file you are generating on the Simulation with the input text file you created for Synthesis.
- Upload the following files to Moodle (an assignment will be created):
  - ✓ VHDL code
  - ✓ VHDL testbench
  - ✓ Input and output text files.